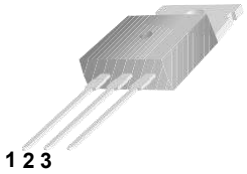
General Description：

150N04 , the silicon N-channel Enhanced VDMOSFETs, is obtained by the high density Trench technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. This device is suitable for use as a load switch and PWM applications. The package form is TO-220AB, which accords with the RoHS standard.

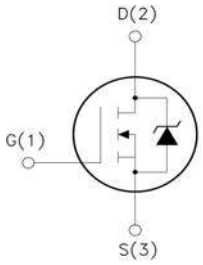
V_{DSS}	40	V
I_D（Silicon limited current）	130	A
P_D	125	W
$R_{DS(ON)Typ}$	3.6	mΩ

TO-220AB



Features：

- **Fast Switching**
- **Low ON Resistance**(Rdson≤5 mΩ)
- **Low Gate Charge**
- **Low Reverse transfer capacitances**
- **100% Single Pulse avalanche energy Test**



1.Gate (G)
2.Drain (D)
3.Source (S)

Applications：

Power switch circuit of adaptor and charger.

Absolute（T_C= 25℃ unless otherwise specified）

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	40	V
I_D	Continuous Drain Current	130	A
	Continuous Drain Current T_C = 100 °C	83	A
I_{DM}[a1]	Pulsed Drain Current	520	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}[a2]	Avalanche Energy	221.1	mJ
P_D	Power Dissipation	125	W
	Derating Factor above 25°C	1	W/℃
T_J， T_{stg}	Operating Junction and Storage Temperature Range	150，–55 to 150	℃
T_L	MaximumTemperature for Soldering	300	℃

Electrical Characteristics（T_C= 25℃ unless otherwise specified）：

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} =40V, V_{GS}= 0V, T_a = 25℃	--	--	1	μA
		V_{DS} =32V, V_{GS}= 0V, T_a = 125℃	--	--	500	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=20V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-20V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=75A	--	3.6	5	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	2.7	4.0	V
Pulse width tp≤300μs, δ ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	--	1	--	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} =25V f = 1.0MHz	--	8900	--	pF
C_{oss}	Output Capacitance		--	550	--	
C_{rss}	Reverse Transfer Capacitance		--	480	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	V_{GS}=10V， R_G=10Ω V_{DD}=30V， I_D=75A	--	48	--	ns
tr	Rise Time		--	88	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	170	--	
t_f	Fall Time		--	62	--	
Q_g	Total Gate Charge	I_D =20A V_{DD} =32V V_{GS} = 10V	--	160	--	nC
Q_{gs}	Gate to Source Charge		--	42	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	33	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	130	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	520	A
V_{SD}	Diode Forward Voltage	I_S=75A,V_{GS}=0V	--	--	1.2	V
trr	Reverse Recovery Time	di/dt=100A/us IF=20A	--	84	--	ns
Qrr	Reverse Recovery Charge		--	75	--	nC
Pulse width tp≤300μs, δ ≤2%						

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Csae	1	℃/W
$R_{\theta JA}$	Junction-to-Ambient	62.5	℃/W

[a1]: Repetitive rating; pulse width limited by maximum junction temperature
[a2]: L=0.1mH,Ias=66.5A Start T_J=25℃

Characteristics Curve：

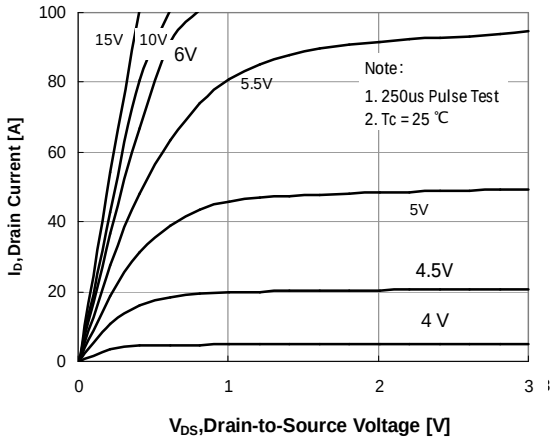


Figure 1. Output Characteristics

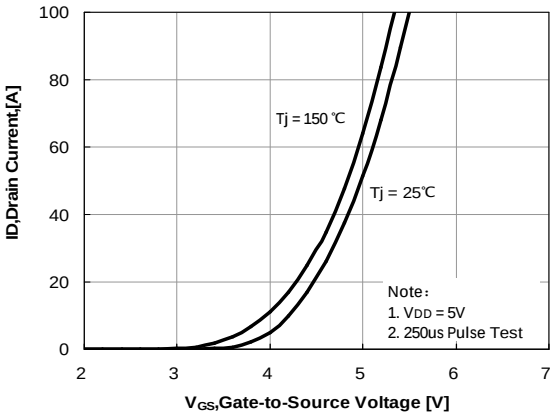


Figure 2.Transfer Characteristics

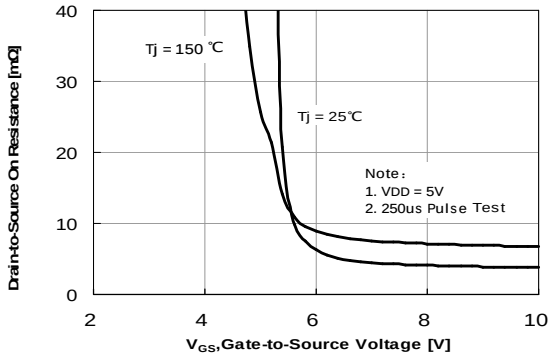


Figure 3. Drain-to-Source On Resistance vs Gate Voltage

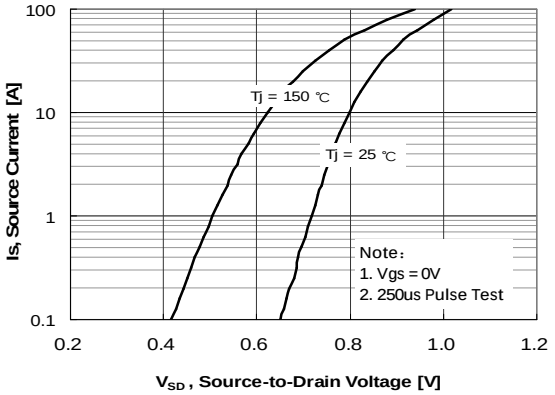


Figure 4. Typical Body Diode Transfer Characteristics

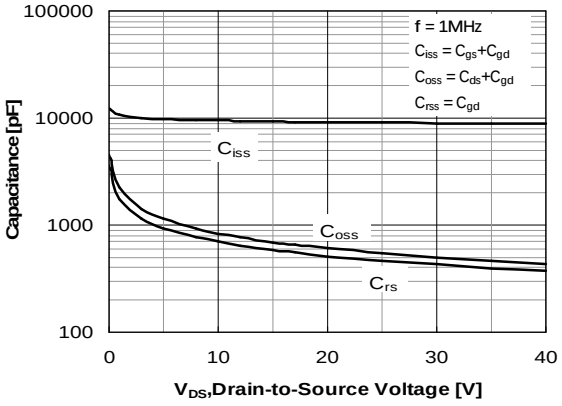


Figure 5. Capacitance Characteristics

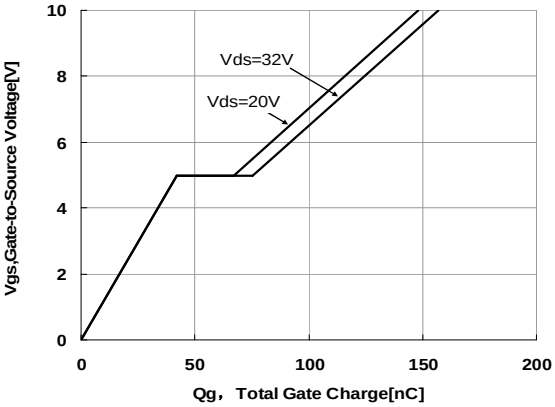


Figure 6. Gate Charge Characteristics

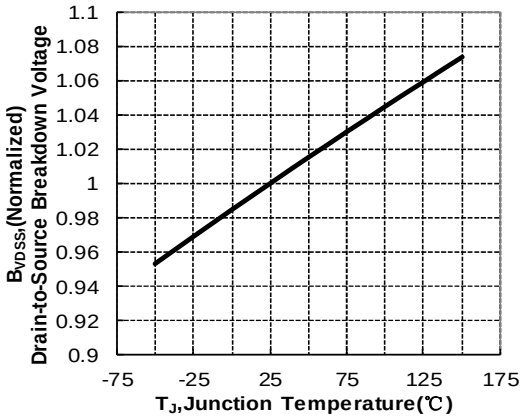


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

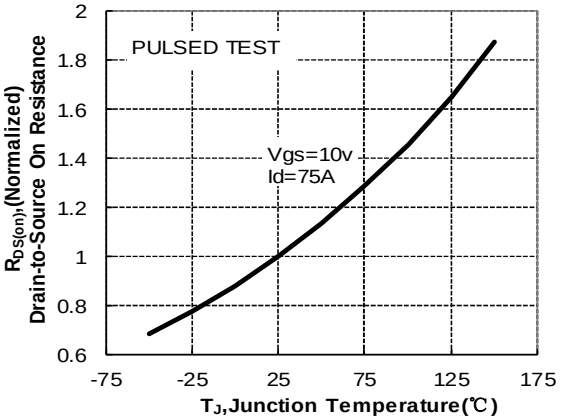


Figure 8. Normalized On Resistance vs Junction Temperature

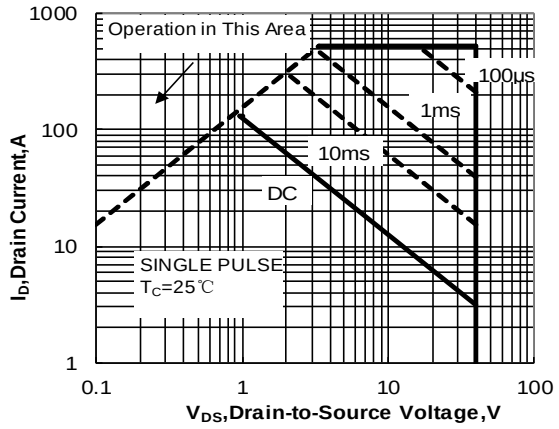


Figure 9. Maximum Safe Operating

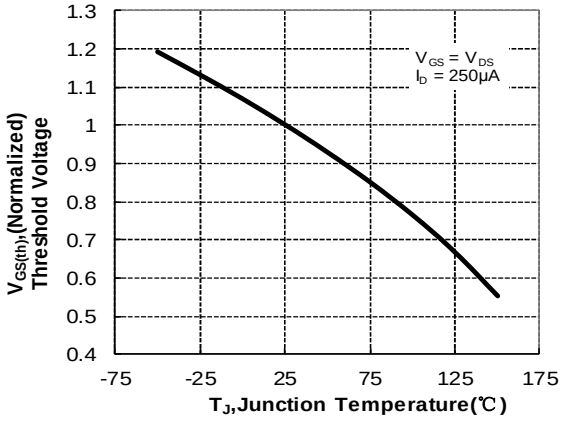


Figure 10. Normalized Threshold Voltage vs Junction Temperature

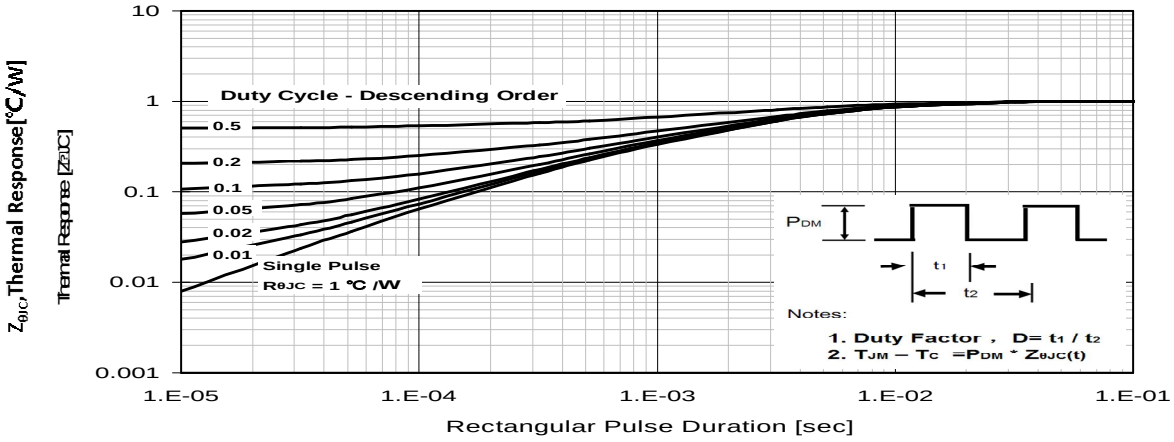


Figure 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Test Circuit and Waveform

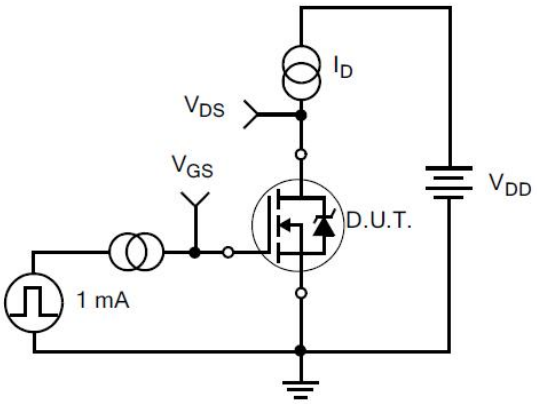


Figure 12. Gate Charge Test Circuit

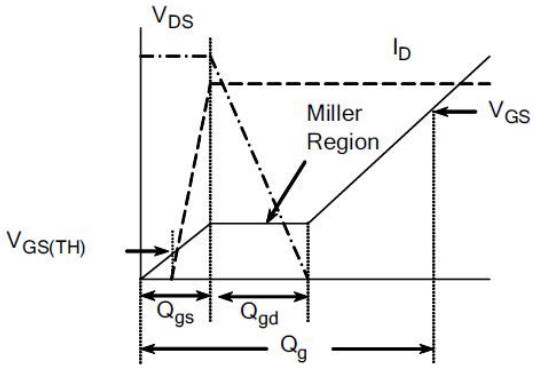


Figure 13. Gate Charge Waveforms

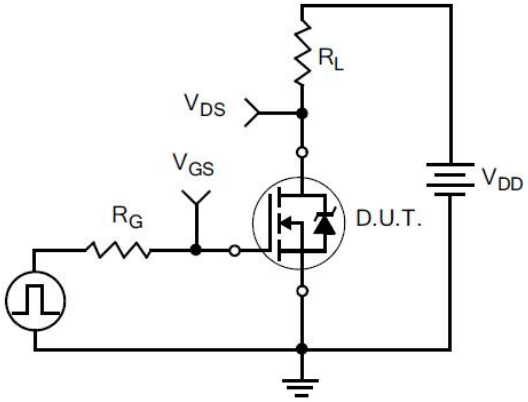


Figure 14. Resistive Switching Test Circuit

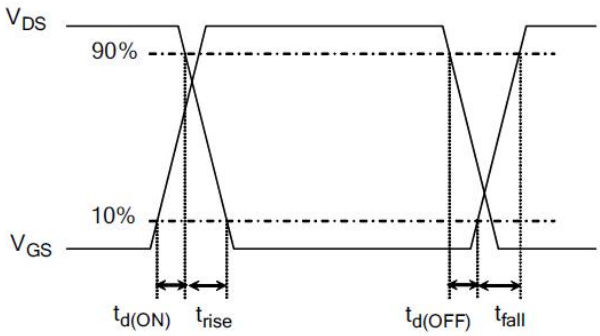


Figure 15. Resistive Switching Waveforms

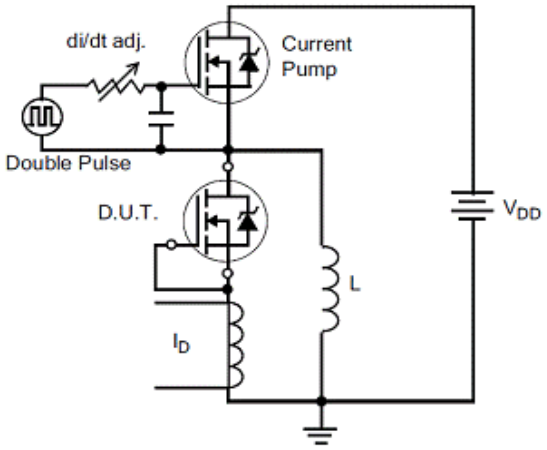


Figure 16. Diode Reverse Recovery Test Circuit

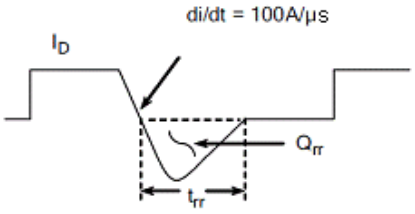


Figure 17. Diode Reverse Recovery Waveform

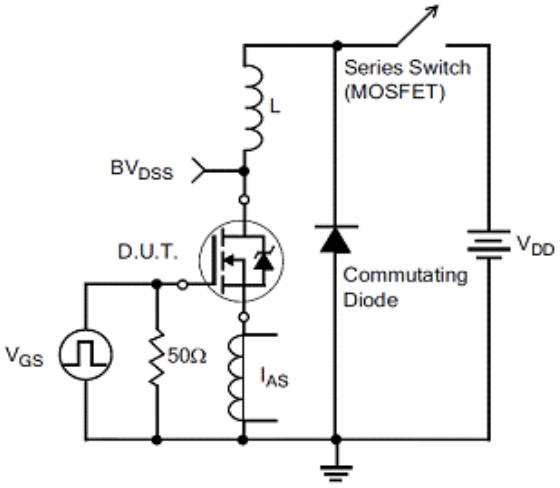


Figure18.Unclamped Inductive Switching Test Circuit

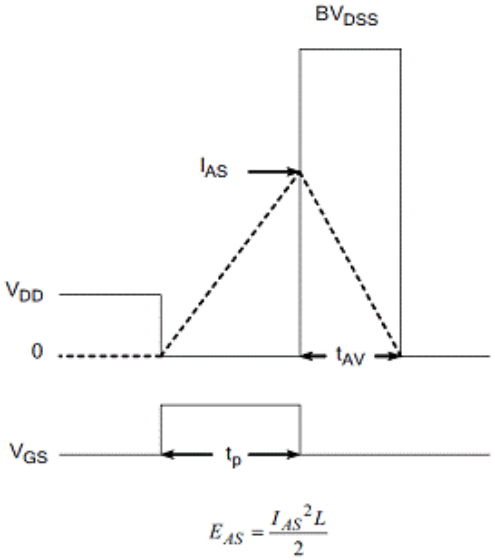
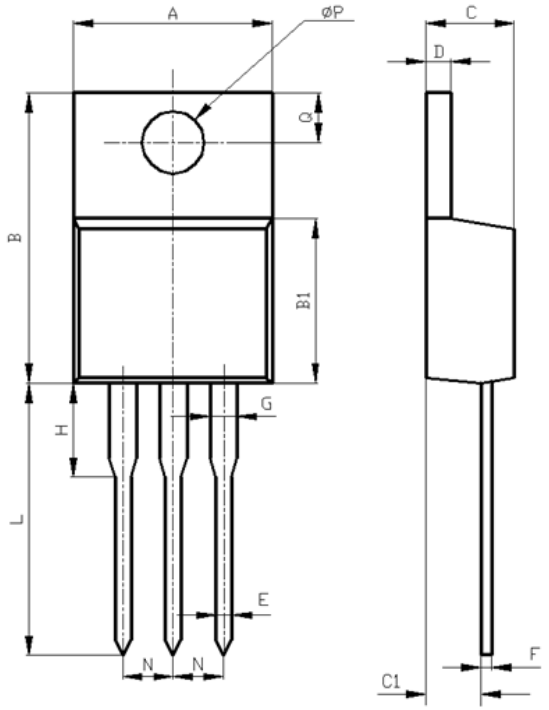


Figure19.Unclamped Inductive Switching Waveform

Package Information：



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L*	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
ΦP	3.50	3.90

*adjustable

TO-220AB Package